CHAPTER 6
TOWARDS THE FUTURE

"Tomorrow will differ from yesterday. It will be new and depend on us. It is to be invented more than discovered"

6.1 VISION

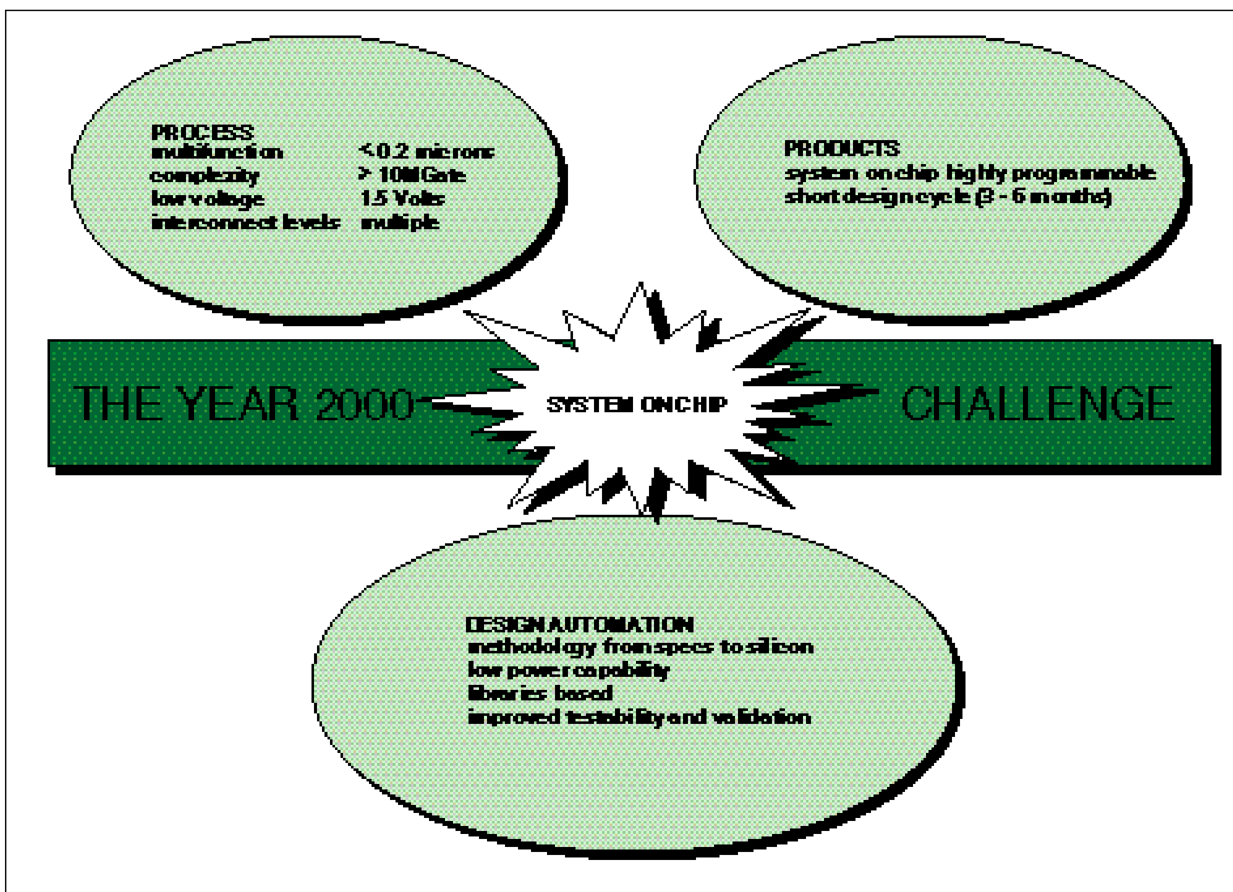
Vision 2000
By the year 2000, be among the top world suppliers and be recognized as the "best-in-class" in service and environmental protection, through strategies and management principles defined in the table opposite.

Vision 2000

- Service and Quality
- Manufacturing
- Globalization
- Innovation
- Strategic alliances
- Product portfolio
- Segment portfolio
- Investments parameters

AND BASED ON MANAGEMENT PRINCIPLES

- TQM (5 key principles)
- Flat organization
- Operational behavior
  (Speed, Focus, Balance, Consistency)



6.2 INNOVATION

During the 1990s the "system-on-chip", integration of a full system or major sub-system on a single chip, has been a new challenge.

The progress of submicron technology has been exponential and research is already delving deeper into submicron technologies. The turnaround time between new product request and chip supply has decreased to the level of a few months.

In parallel with function integration, package technology has been progressing. Packages with more than 500 pins and lead pitch smaller than 0,25 mm have been developed under special package programs such as Chip Size Package (CSP) and Ball Grid Array (BGA).

Advanced technologies allow concurrent test development during the chip design stage. Improvements in final testing are constantly being studied (see) the Cause and Effect diagram on the next page and Design for Testability (DFT) below.

Progress towards "System-on-Chip" requires integration on a single chip of functions that previously were shared among different chips and realized with different technologies. Combination on a single chip of different technologies generates new failure mechanisms and new reliability challenges.

6.3 JOINT COOPERATION FOR RESEARCH

To guarantee continuous technological development and to offer leading edge products, SGS-THOMSON invests significantly in Research and Development every year. Resources needed for independent development of new processes are however prohibitively large for a single semiconductor manufacturer.

Partnership agreements and sharing of know-how are common practice in the semiconductor industry, particularly for high-risk and costly advanced research programs.

DESIGN FOR TESTABILITY
Using built-in self test and IDDq test

Complex digital products like microcontrollers, MPUs, ASICs and mixed signal devices are designed using various techniques that allow the highest level of fault identification. Fault detection systems are designed into the product rather than implemented in test as an after thought. Using the built-in self test approach, special test structures are included in the design.

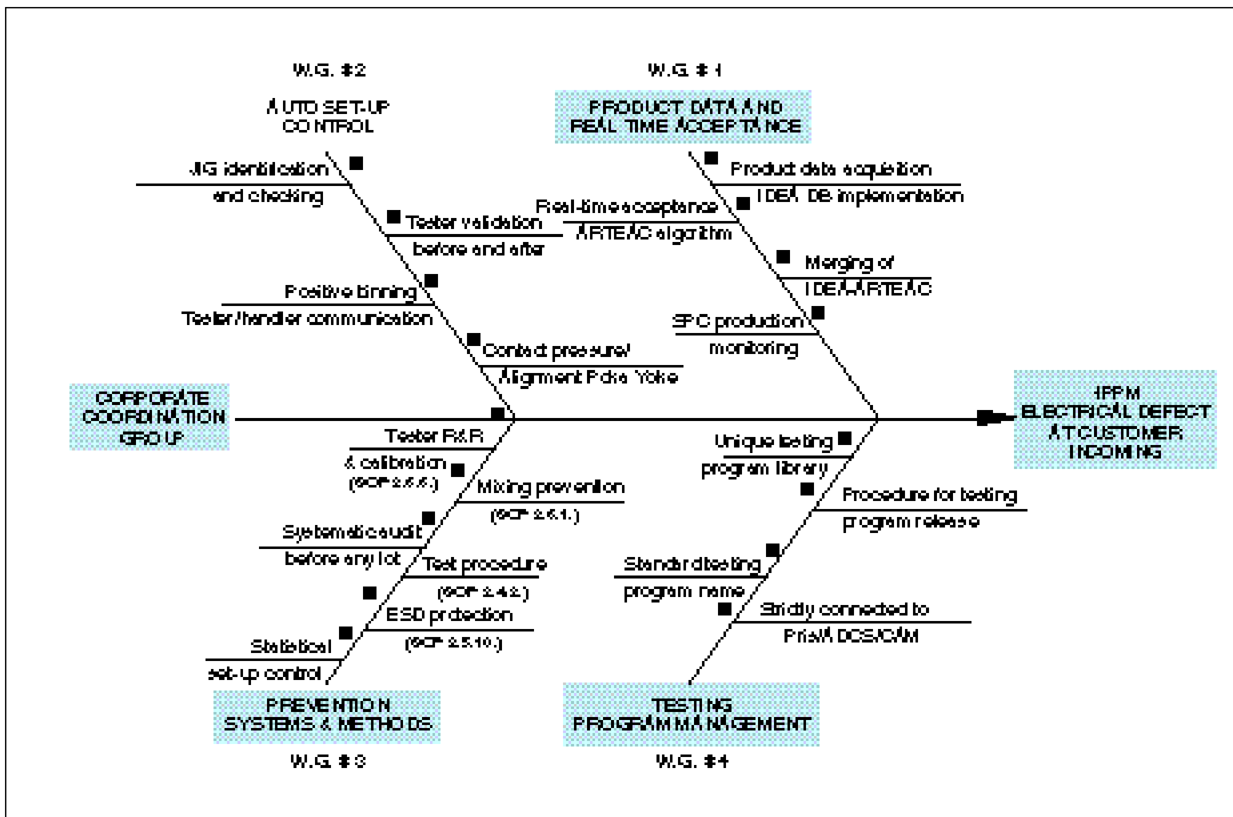
This improves the test coverage which is measured during design simulation and provides a detection of faults at electrical test that are not usually found by functional testing regardless of its thoroughness. Detection of faults, "stuck at 1 or 0" using this approach of design for testability is not always sufficient to ensure the maximum test efficiency and consequently good quality products.

Another technique used at electrical test is the IDDq test method. Its purpose is to improve the level of fault detection in conjunction with the "stuck at 1 or 0" fault graded test vectors.

This method consists of a power supply current measurement in the quiescent state of the device. It detects small changes in leakage current which indicate problems such as "soft shorts", and "soft metal bridging". It is particularly efficient in detecting gate oxide shorts, interlayer shorts, electromigration, filament growth, ESD and EOS degradation, latch-up, scratches and contamination.

The majority of these type of defects are generally eliminated during a burn-in process or during a high stress electrical test. The IDDq test is not however used to replace burn-in or any other test. It reduces them and also avoids the assembly of bad parts. It also improves the total observability of faults, assists in device debugging and in-line device failure analysis.

The use of Design for Testability (DFT) combined with IDDq testing techniques is the preferred way to detect all the potential functional and reliability defects. Both DFT and IDDq are now Company standard tests.



Cause and effect study of all factors that contribute to electrical testing performance

SGS-THOMSON's policy for global cooperation in R & D has three categories:

- horizontal cooperation with European and non-European competitors
- joint R & D Centers
- strategic alliances with key customers and suppliers.

A list of published technical literature and conference papers are summarized in the appendix.

European Community Program for R & D Micro-Electronics Development for European Applications (MEDEA), a pan-European program of advanced research and development, designed to ensure Europe's continued industrial competitiveness into the next century has been endorsed by the European Research and Development Program Group (EUREKA).

MEDEA brings together many of Europe's top electronics companies in a five year program. The importance of MEDEA lies in the growing role that microelectronics is playing in key industries such as computers, automobiles, telecommunications systems and consumer equipment.

The proportion of electronic systems that can be integrated into silicon chips is rising rapidly, giving an increasing advantage to equipment manufactures who can make early use of the most advanced semiconductor technologies.

Joint R & D Centers
Public support, European programs, and joint cooperation emphasize the convenience of sharing the work in joint R&D Centers, where partners' researchers work together.

A typical example is the Crolles center, close to Grenoble, encompassing R&D activity based upon the "GIE Centre Commun", a joint venture between SGS-THOMSON and France Telecom on one hand, a specific partnership between SGS-THOMSON and Philips Semiconductor on the other hand, together with a manufacturing unit operated by SGS-THOMSON.

It combines in a single 8" wafer fab, the resources for advanced technologies development, pilot prototyping and volume production.

In addition advanced research benefits from the joint forces of the "Commiiariat a l'Energie Atomique (CEA-LETI) and France Telecom in the Grenoble area.

Highly complex integrated circuits for specific applications, including telecommunications, consumer, computers and automotive, are manufactured using submicron technologies. The installation will enable technologies to the 0.18 micron generation.

Ongoing activities in the field of advanced technology and product development are:

- Fuzzy logic processors
- very high speed bipolar technology (more than 20 GHz)
- vertical intelligent power ICs
- advanced microprocessors.

6.4 ADVANCED TECHNOLOGIES IN PACKAGING

Due to the exponential progress of silicon technology and nearly continuous requests from semiconductor users for higher performance in packaging, progress in package state of the art must be as fast as the requirement evolution.

Needs for higher performance are mainly:

- speed increase (decreasing parasitic impedance of internal connections)
- power dissipation increase
- increase of package efficiency (ratio between chip area and package area)
- increase of pin count and finer pitch
- Multichip Modules (MCM).

SGS-THOMSON is following different roadmaps for package development depending on the family of products involved.

Signal Packages Low Pin Count (< 100 pins)
A typical example of chip family involvement is programmable memories.

Package size reduction and finer lead pitch are key priorities.

Changing from Dual-in-Line Plastic (DIP) to Shrink Small Outline Package (SSOP) or Plastic Quad FlatPack (PQFP) package provide space efficiency increases from 1-3% to 15-30% and pitch decreases from 2,54 mm to 0,5-1 mm.

The trend is towards Chip Size Package (CSP) with package size close to chip size.

ASIC and Dedicated Integrated Circuits
Pin count, clock frequency and power dissipation are preeminent features. Ball Grid Array (BGA) with multilayer frame is an ideal solution because it will allow pin count up to 1000 pins, clock frequency up to 250 MHz and power dissipation up to 20-30 watts.

In addition solder balls eliminate lead coplanarity problems. They are located on the bottom of the package, rather than leads arranged round the package sides and allow comparable pin count in less occupied area compared with Quad Flat Pack.

Power Devices
For this family, large chip, high power dissipation and decrease in package size, are preeminent features.

New developments are:

- Maxiwatt, package size TO220 with possibility of mounting the same chip size as SOT93
- D-PACK and D2-PACK for surface mounting of transistors
- Power-SO up to 36 pin and power QUAD up to 64 pin (copper internal heatsink, soft die attach and high diameter wires for high current).

APPENDIX A

SOME SGS-THOMSON TECHNICAL LITERATURE AND CONFERENCE PAPERS REFLECTING CONTRIBUTIONS TO THE ADVANCEMENT OF SEMICONDUCTOR QUALITY AND RELIABILITY

TITLE	AUTHOR	PUBLICATION/CONFERENCE
Reliability issues of flotox EEPROM cells.	C. Papadas	Materials Science & Engineering Report: a Review Journal, 1995
Modeling of the intrinsic retention characteristics of flotox EEPROM cells under elevated temperature conditions.	C. Riva F. Pio P. Ghezzi C. Papadas G. Pananakakis G. Ghibaudo	IEEE Transactions on Electron Devices, 1995
Reliability issues of furnace nitridated oxides prepared with reduced thermal budget in N2O ambient.	E. Vincent C. Papadas	Solid State Journal, 1995
Inter-metal dielectric planarization process for 0.35 micron multilevel interconnection devices.	M. Bacchetta C. Zaccherini L. Zanotti	Applied Surface Science, 1995
Non-local effects in p-mosfet substrate hot-hole injection experiments.	R. Bez L. Selmi E. Sangiori	IEEE Electron Device Letters, Vol. 16, No. 10, 1995
Physical model of threshold voltage in Si MOS transistors including reverse short channel effect.	H. Brut A. Juge	Electronic Letters, 1995
Bimodal use of body bias for leakage elimination (Bubble).	L. Baldi	Alta Frequenza, 1995
Stripping hall effect studies in Annealing kinetics of defects in ion-implanted semiconductors.	M.L. Polignano G. Queirolo	Book chapter: edited by C. Christfides & G. Ghibaudo, Academic Press, San Diego
Modeling of the retention characteristics of Flotox EEPROM cells.	C. Papadas G. Pananakakis	Transactions on Electron Devices, 1995
Observation of two types of trapping centers in thin film transistors using charge pumping technique.	A. Balasinski J. Worley K.W. Huang J. Walters F.T. Liou	IEEE Electron Device Letters, 1995
SIA roadmap: Una sfida per L'industria dei semiconduttori.	G. Zocchi	Alta Frequenza, 1995
A model for hot-electron and hot-hole injection in flash EEPROM programming.	F. Piccinini G.L. Mei R. Bez C. Lombardi A. Concannon A. Mathewson	Microelectronics Journal, 1994
Impact of furnace nitridation time in N^2O ambient on the quality of the Si/SiO^2 system.	F. Pio C. Riva C. Papadas R. Le Bihan E. Andre-Benoit	Microelectronics Journal , 1994
Correlation between substrate hot electron energy and homogeneous degradation in n-mosfets.	R. Bez L. Selmi C. Fiegna	IEEE Transac. on Electron Devices, 1994

TITLE	AUTHOR	PUBLICATION/CONFERENCE
Impact of the furnace nitridation time in N^2O ambient on the quality of the Si/SiO^2 system.	R. Le Bihan C. Papadas	Elsevier Advanced Technology, (Microelectronic Journal), 1994
The endurance performance of flotox EEPROM cells with WSi^2 overcoated floating gate electrode.	F. Pio C. Riva P. Ghezzi C. Papadas G. Ghibaudo G. Pananakakis	Microelectronics Journal, 1993
Electrical characterisation and reliability of double doped drain MOS transistors compatible with an EEPROM process.	L. Fratin C. Riva B. Vaiana P. Pavan E. Zanoni	Microelectronics Journal, 1993
Wafer level tunnel oxide reliability evaluation by means of the exponentially ramped current stress method.	P. Cappelletti P. Ghezzi F. Pio C. Riva	Microelectronics Reliability, 1993
Reliability simulations of the endurance performance of flotox Eprom cells using Spice.	F. Gigon P. Mortini	Quality & Reliability Engineering, 1993
Reliability issues of silicon dioxide structures application to flotox EEPROM cells.	C. Papadas	Journal of Microelectronics of Reliability, 1993
Influence of rapid thermal nitridation process in N^2O ambient on the endurance performance of flotox EEPROM cells.	C. Papadas P. Mortini	IEEE Electronic Letters, 1993
Moisture absorbtion and pop corn risk on plastic ball grid array.	L. Herard	IEE Computer Pack Workshop, Tsukuba, Japan, 1996
Reliability improvements of die attach by means of Acoustic Microscopy.	V. Motta R. Tiziani V. Del Bo	International Acoustic Micro Imaging symposium, IAMIS & Sonoscan Inc, San Diego, 1996
Evaluation of low stress IC encapsulation for multichip module and single chip package applications.	A. Saoui R. Doyle J. Barret	Internation Flip Chip, Ball Grid Array, Tab and Advanced Packaging Symposium, Sunnyvale, 1996
Degradation mechanism of flash cell induced by parasitic drain stress conditions.	R. Bez D. Cantarelli L. Fratin G. Mei P. Cappelleti	4th Non Volatile Semiconductor Memory Workshop, NVSMW, San Francisco, 1995
Rapid Thermal Processing (RTP) impact on thin gate oxides.	G. Ghidini N. Bellafiore	3rd International Rapid Thermal Processing, RTP, Conference, Amsterdam,1995
A new method to statistically monitor active area spread and oxide thinning in real devices.	G. Ghidini	Integrated Reliability Workshop, IRW, Lake Tahoe, 1995
Passivation scheme impact on retention reliability of non volatile memory cells.	R. Bottini A. Cascella F. Pio B. Vajana	Integrated Reliability Workshop, IRW, Lake Tahoe, 1995
Metal contamination in ion implantation processes.	M.L. Polignano C. Bresolin F. Cazzaniga G. Queirolo	International Conference on Ion Implantation Technology, Catania, Italy, 1995
Investigation of metal contamination by photocurrent measurements.	M.L. Polignano C. Bresoli F. Cazzaniga G. Queirolo	Society Photo-optical Instrument Engineers, SPIE Microelectronics Manufacturing, Austin, Texas, 1995

TITLE	AUTHOR	PUBLICATION/CONFERENCE
Purity issues in chemicals and gases: or how pure is pure enough.	A. Tonti	SEMICON Europe, Geneva, 1995
Electrical characterization of highly reliable 80 Angstrom oxide.	G. Ghidini	Meeting of the Electrochemical Society, Los Angeles, 1995
A non destructive technique, thermal-wave imaging to characterize the electromigration of Al alloy.	A. Brun M. Marty	7th Symposium on Non destructive Characterization of Materials, Prague, 1995
The impact of negative overlap between metal and via levels on via performance.	W. Deodel E. Rouchouze	Advanced Mutualization & Interconnect Systems for VLSI Applications, 1995
Linewidth influence on electromigration tests at wafer-level on TiN/AlCu/TiN/Ti metal lines.	F. Giroux H. Roede	Society Photo-optical Instrument Engineers, SPIE, Microelectronics Manufacturing, Austin, Texas, 1995
New approach in scanning electron microscopy resolution evaluation.	H. Martin P. Perret	Society Photo-optical Instrument Engineers, SPIE, Santa Clara, 1995
Accurate prediction of PQFP warpage.	A. Saboui G. Kelly	International Society for Hybrid Manufacture,Las Vegas, 1995
Monitoring of metallic contamination by direct and indirect analytical methods.	P. Patruno	SEMICON West, San Francisco 1995
Reliability and characterization of ultra thin dielectric films using F-N injection experiment.	A. Straboni O. Briere V. Thirion K. Barla	Insulated Films on Semiconductors, INFOS, Villard de Lans, France, 1995
On-line characterization of metallic microcontamination for ULSI microelectronics.	D. Walz J.P. Joly G. Kamarinos K. Barla	European Solid State Device Research Conference, ESSDERG, The Hauge, 1995
Wafer-level electromigration tests on NIST and SWEAT structures.	F. Giroux C. Gounelle P. Mortini	IEEE International Conference on Microelectronic Test Structures, ICMTS, Japan, 1995
Degradation features of poly-emitter npn BJTs after hot carrier injection.	F. Maugain C. Papadas N. Gambetta P. Mortini	IEEE International Reliability Physics Symposium, IRPS, Las Vegas, 1995
Threshold voltage after hot carrier injection on deep submicron N-channel mosfets - A quasi uniform approach.	C. Papadas N. Revil E. Vincent	Insulated Films on Semiconductors, INFOS, Villard de Lans, France, 1995
Impact of I/O buffer configuration on the ESD performance of a 0.5 micron CMOS process.	T. Nikolaidis C. Papadas P. Mortini	Electrical Overstress / Electrostatic Discharge Symposium, Phoenix, 1995
ESD electrothermal simulation of LDD-formed zener diodes.	T. Nikolaidis H. Jaouen P. Mortini	European Symp., Reliability of Electron Devices, ESREF, Arcachon, France, 1995
New standards for thermal measurements.	V. Motta	Thermal Management of Electronic Systems, Eurotherm Seminar, Leuven, 1995
Thermal characterization of a multi layer 313 Plastic Ball Grid Array device.	J. Blair B. Bond B. Freyman M. Hundt V. Motta	Flipchip, BGA, and TAB Symposium, ITAB, San Jose, 1995
Thermal impedance evaluation with different Power Profiles.	V. Motta C. Villa T. Zhou	Thermal Management of Electronic Systems, Eurotherm Seminar, Leuven,1995

TITLE	AUTHOR	PUBLICATION/CONFERENCE
Surface treatment for plastic ball grid array assembly and its affect on package reliability.	L. Herard	Workshop on Flip Chip & BGA, Berlin, 1995
Metal contamination in ion implantation processes	M.L. Polignano G. Queirolo C. Bresolin F. Cazzaniga	Ion Implantation Technology, Catania, Italy, 1994
A Test pattern to investigate the effect of capping layers on the hot carrier induced photon spectra of MOSFETS.	R. Bez M. Lanzoni L. Selmi M. Manfredi	International Conference on Microelectronic Test, ICMTS, San Diego, 1994
A test chip and an accurate measurement system to characterize hot hole injection in the gate oxide of p-MOSFETs.	R. Bez L. Selmi E. Sangiorgi B. Ricco	International Conference on Microelectronic Test, ICMTS, San Diego, 1994
An electrical stress test to monitor single bit failures in Flash-EEPROM structures.	P. Cappelletti R. Bez D. Cantarelli L. Ravazzi	IEEE, Non-Volatile Memory Workshop, NVMW, Monterey, 1994
Applications of a novel hot carrier injection model in Flash EEPROM design.	F. Piccinini G.L. Mei R. Bez C. Lombardi A. Concannon A. Mathewson	Device Researc European Solid State Conference, ESSDERC, Edinburgh, 1994
Experimental analysis of polarization in hot carrier luminescence of silicon devices.	R. Bez L. Selmi A. Pieracci M. Lanzoni M. Pavesi E. Sangiogi	European Solid State Device Research Conference, ESSDERC, Edinburgh, 1994
Failure mechanisms of Flash cell in program/erase cycling.	P. Cappelletti R. Bez D. Cantarelli L. Fratin	International Electron Devices Meeting, IEDM. San Fransisco, 1994
A reliability simulator for the retention characteristics of EEPROM cells under elevated temperature conditions.	C. Riva F. Pio P. Ghezzi C. Papadas G. Pananakakis G. Ghibaudo	Non Volatile Semiconductor Memory Group, NVMSG, Monterey, 1994
Impact of surface nitridation temperature in N2O ambient on the quality of the Si/Sio2 system.	F.Pio C. Riva C. Papadas	European Solid State Device Research Conference, ESSDERC, Edinburgh, 1994
Sheet resistance and layout effects in accelerated tests for dielectric reliability evaluation.	F. Pio	6th ESPRIT Workshop on Characterization and Growth of Thin Dielectric, Cork, 1994
Integrated circuit metrology, inspection and process control IV.	H. Martin	Society Photo-optical Instrument Engineers, SPIE, San Jose, 1994
A reliability simulator for the retention characteristics of Flash EEPROM cells under elevated temperature conditions.	C. Papadas	Non Volatile Semiconductor Memory Group, NVMSG, Monterey, 1994
Current and temperature distribution impact on electromigration failure location in SWEAT structure.	F. Giroux C. Gounelle N. Vialle P. Mortini	International Conference on Microelectronics, Test Structures, ICMTS, San Diego, 1994

TITLE	AUTHOR	PUBLICATION/CONFERENCE
Simulation of hot carrier degradation phenomena in n-MOSFETs with a 2D device simulator.	M. Diaz Nava	6th ESPRIT Workshop on Thin Dielectrics in Microelectronics, Cork, 1994
Electrical Measurement and Modelling of High Pin Count Package for High Speed logic.	A. Castellane R. Evans C.M. Villa	International Society for Hybrid Manbufacturing, ISHM Nordic, Helsinki, 1994
Mastering key factors which affect flash memory reliability.	P. Cappelletti L. Ravazzi A. Panchieri	European Symp. Reliability of Eletron Devices, ESREF, Bordeaux, 1993
A transient reliability simulator for the retention characteristics of Flotox EEPROM cells.	C. Riva F. Pio P. Ghezzi C. Papadas G. Pananakakis G. Ghibaudo	European Symp. Reliability of Eletron Devices, ESREF, Bordeaux, 1993
Measurement of the hot hole injection probability from Si into SiO2 in p-MOSFETs.	R. Bez L. Selmi E. Sangiori B. Ricco	International Electron Devices Meeting, IEDM, Washington, DC, 1993
Volume and interface degradation features of n-channel MOSFETs after uniform hot carrier injection.	C. Papadas N. Revil P. Mortini	Symposium on VLSI Technology, Tokyo, 1993
Investigation of hot carrier induced degradation in 0.1 micron channel length n-MOSFETs.	N. Revil P. Mortini	Insulated Films on Semiconductors, INFOS, Delfi, 1993
The threshold voltage shift after hot carrier injection on submicron n-channel MOSFETs.	N. Revil C. Papadas H. Dubreuil P. Mortini	European Solid State Device Research Conference, ESSDERC, Grenoble, 1993
Temperature measurements on metallic lines under current stress by laser probing and correlation with electromigration tests at wafer level.	F. Giroux C. Gounelle P. Mortini	Society Photo-optical Instrument Engineers, SPIE, Monterey, 1993

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